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Highly Reliable Quadruple-Node Upset-Tolerant D-Latch

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Abstract *Web-page recommendation plays an important role in intelligent Web systems. Useful knowledge discovery from Web usage data and satisfactory knowledge representation for effective Web-page recommendations are crucial and challenging. This paper proposes a novel method to efficiently provide better Web-page recommendation through semantic-enhancement byinte grating the domain and Web usage knowledge of a website. A number of effective queries have been developed to query about these knowledge bases. Based on these queries, a set of recommendation strategies have been proposed to generate Web-page candidates. The recommendation results have been compared with the results obtained from an advanced existing Web Usage Mining (WUM) method. The experimental results demonstrate that the proposed method produces significantly higher performance than the WUM method.Many kinds of research have shown that people are more likely to trust each other with the same attitude toward similar things. In this paper, we consider seeking and accepting sentiments and suggestions in E-commerce systems somewhat implies a form of trust between consumers during shopping. Following this view of point, an E-commerce system reviews mining oriented sentiment similarity analysis approach is put forward to exploring users' similarity and their trust. We divide the trust into two categories, namely direct trust, and propagation of trust, which represents a trust relationship between two individuals. The direct trust degree is obtained from sentiment similarity, and we present an entity-sentiment word pair mining method for similarity feature extraction.*

1. INTRODUCTION

As CMOS technology scaling pushes towards the reduction of the length of transistors, electronic circuits face numerous reliability issues, and in particular nodes of D-latches at nano-scale confront multiple-node upset errors due to their operation in harsh radiative environments. In this manuscript, a new high reliable D-latch which can tolerate quadruple-node upsets is presented. The design is based on a low-cost single event double-upset tolerant (LSEDUT) cell and a clock-gating triple-level soft-error interceptive module (CG-SIM). Due to its LSEDUT base, it can tolerate two upsets, but the combination of two LSEDUTs and the triple-level CG-SIM provides the proposed D-latch with remarkable quadruple-node upsets (QNU) tolerance. Applying LSEDUTs for designing a QNU-tolerant D-latch improves considerably its features; in particular, this approach enhances its reliability against process variations, such as threshold voltage and (W/L) transistor variability, compared to previous QNU-tolerant D-latches and double-node-upset tolerant latches. Furthermore, the proposed D-latch not only tolerates QNUs, but it also features a clear advantage in comparison with the previous clock gating-based quadruple-node-upset-tolerant (QNUTL-CG) D-latch: it can mask single event transients. Specific figures of merit endorse the gains introduced by the new design: compared with the QNUTL-CG D-latch, the improvements of the maximum standard deviations of the gate delay, induced by threshold voltage and (W/L) transistors variability of the proposed D-latch, are 13.8% and 5.7%, respectively. Also, the proposed D-latch has 23% lesser maximum standard deviation in power consumption, resulting from threshold voltage variability, when compared to the QNUTL-CG D-latch.

Index Terms - Power-delay product (PDP), soft errors (SE), single event upset (SEU), high impedance state (HIS), single event transient (SET), dual interlocked storage cell (DICE), triple path DICE (TPDICE), quadruple-node upsets (QNUs).

Introduction

Nano-scaling integrated circuits and systems rises a sensitivity challenge to soft errors generated by radiation-induced charges when the size of the transistors is reduced . There are different designs of hardened D-latch against soft errors such as single-node upsets and double-node upsets (resulting from a striking particle injected to double nodes). Furthermore, the reduction of transistor size can cause a striking particle to affect multiple nodes (more than two). This effect can cause multiple-node upsets (MNUs), leading to triple-node upsets and quadruple node upsets . This represents a huge concern to design reliable storage modules, especially for their safe application when used in harsh radiative environments . There is a lot of investment in hardened circuit structures to reduce the side effect of soft errors. These circuits comprise memory cells flip-flops and latches . But yet most of the existing hardening

approaches face limitations; for example, some hardened D-latches cannot recover reliably after flipping, even if the output node stores its value.

Previous Hardened D-Latches

A.DICE

Many techniques have been presented to mitigate SNU in D-latches and among those hardened D-latches, DICEs are very effective [26]. In Fig. 1(a), the schematic of a DICE structure is shown. This structure can recover from any SNU and it is self-recoverable to the DNUs in some nodes.

B.CLCT

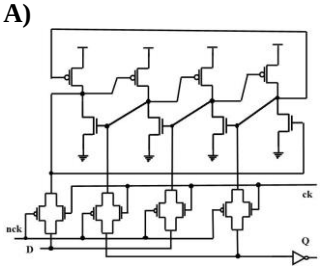
Circuit and layout combination technique (CLCT), which is shown in Fig. 1(b),

operates based on clock-gating technology, in which there are not positive feedback loops of its DICE in the transparent mode to prevent current competition in the output node [15]. The data at holding time can be retained in the DICE and keeper; then can be transferred to the output by a C-element tolerating both SNU and Single Event Double-Upset (SEDU).CLCT [15] has a high impedance state in the output node when SNU or SEDU take place; for example, when SNU happens in the keeper or SEDU happens in CG-based DICE, the output goes to a high impedance state. Also, this D-latch is not fully hardened against SEDU.

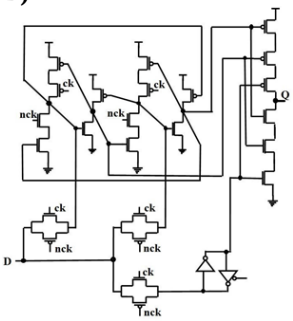
C.TPDICE-BASED D-LATCH

Triple path DICE (TPDICE) is a hardened D-latch alternative with immunity against SET, SNU, DNU, and a HIS insensitivity [27], which is shown in Fig. 1(c). In this structure, a TPDICE is used for retaining the data in holding time; furthermore, it includes a three-input C-element for filtering SEDU, an embedded Schmitt trigger inverter (STI) for filtering the SET in the transparent path, and a keeper for avoiding a high impedance state in the output node

A)



B)



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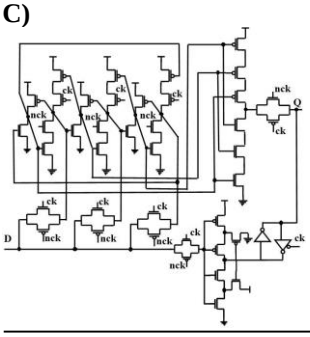

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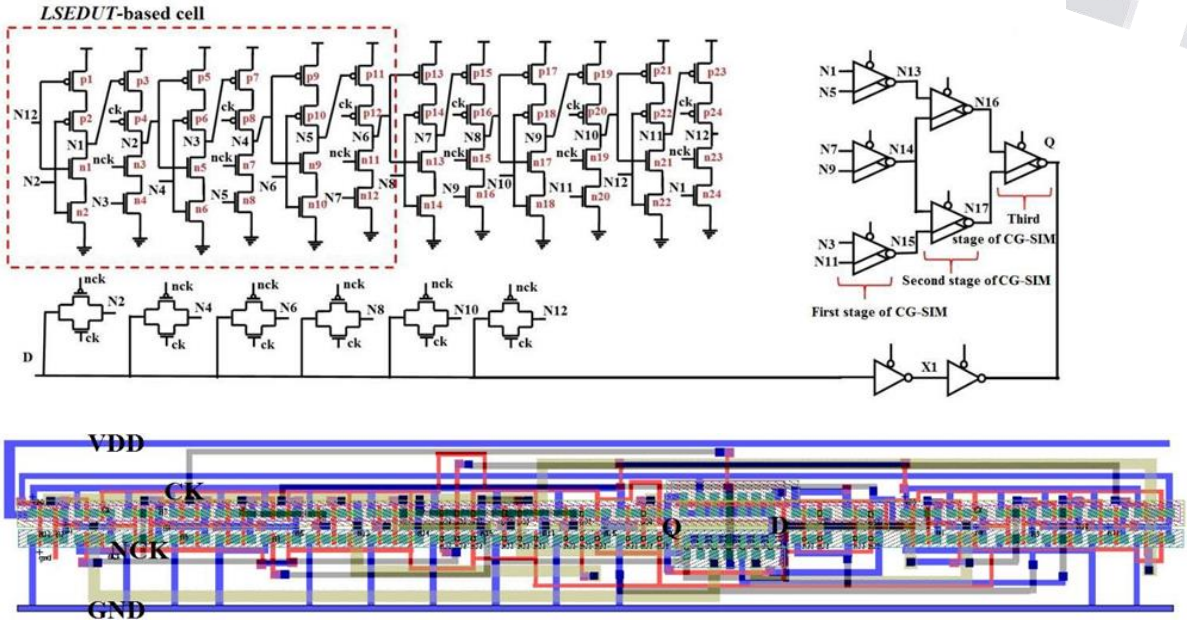
Proposed D-Latch

Fig. 2(a) shows the LSEDUT-based proposed D-latch with triple-level CG-SIM and two CG-inverters to filter SET in transparent mode. The layout of the device is shown in Fig. 2(b). In this latch, D and Q are the input and output; ck and nck are the clock circuit and inverter clock circuit rails, respectively. When ck 1, nck 0, the latch works in the transparent mode and the gate of transistors connected to N2, N4, N6, N8, N10, N12, and Q are charged or discharged by the D input through transmission gates. Then, the D input propagates through six 2-input C-elements and stablishes the values of N1, N3, N5, N7, N9, and N11. In the transparent mode, the positive feedback of the LSEDUT part is not active,and the triple-level CG-SIM is not connected to the output node to avoid current competition, which also decreases power consumption and delay. Moreover, this hardened D-latch has SET-filtering feature in transparent mode. If a SET arrives at D from a previous combinational part before the D-latch, it will pass through the CG-inverter and will arrive at x1 node reversing the SET. Then, by passing through the second CG-inverter and achieving the Q node, the SET is filtered by the delay introduced by these two inverters. For example, if SET comes and D becomes low, a positive SET (low-high-low) at x1 will appear. But, the right value of x1 is low and the NMOS transistor of the second inverter is off. Therefore, the value of Q cannot change until x1 becomes high, which needs time to charge the NMOS capacitors of the second inverter. In the transparent path, these two CG- inverters are applied to introduce delay for filtering the SET. In the latching time, when ck=0 and nck=1, N2, N4, N6, N8, N10, N12, and Q are disconnected from the D input, however, two LSEDUTs with triple-level CG-SIM are connected to Q. This implies that Q is driven by a triple-level CG-SIM instead of the D input in the transparent path. Additionally, the feedback loops of each LSEDUT are activated to hold values. Therefore, the proposed D-latch can properly store values and drives valid values to the output node (Q). The output node does not present any HIS in the holding time when SNU, DUN, TUN, or QUN take place.It is worth mentioning that the triple-level CG-SIM has three stages CG-3 input C-elements, which are less power demanding, but as this part does not connect to Q in transparent mode, the values of N13, N14, N15, N16, N17 are floating.If any particle strikes at any node of the proposed D-latch as one SNU, this structure is self-recoverable like an LSEDUT latch. In the following subsections, we cover different situations where different levels of upsets occur at different nodes of the proposed D-latch and its immunity is systematically evaluated.



b

Proposed D-latch (a) schematic, (b) layout.

Immunity Against Snu

Since the proposed design is very symmetric, N1, N3, N5, N7, N9, and, N11 have the same value (inverted input data) and N2, N4, N6, N8, N10, and N12 have the same value as the input value. Also, N13, N14, N15 have the same value as the input value (D-input passes through two inverters), and N16, N17 present the same value as the inverted value of the input. So, five different cases (e.g.,

N1, N2, N13, N16, and Q) should be investigated for a SNU. For the internal nodes of the LSEDUT, N1 or N2, if one of them suffers from a SNU, for example, N1 is affected when D 0 (N2 0, N1 1), then it will be discharged to 0, p3 is turned one, and N2 becomes unstable, but this charge cannot make N2 turn into high level, because n4 is ON; as the result, N1 and N2 can be recovered by N12 and N3, respectively. Even, if this charge is

large enough to change the value of N2, it will be filtered by the tripe-level CG-SIM. This SNU cannot affect the output of the proposed D-latch. If any SNU affects the N2 node, the analysis of recovery is the same as for N1. When N13 or N16 are affected by SNU, as they are derived by LSEDUTs connected to the first stage of the CG-SIM, they can recover their value. If Q is affected by a SNU, it will flip temporarily, but as the LSEDUTs and the triple-level CG-SIM save their values and they are not affected by the SNU, therefore, Q will be recovered. As a summary, the proposed D-latch is immune against any SNUs.

Immunity Against Dnu

After evaluating against SNU, the immunity of the proposed D-latch against DNU is considered. As this circuit is symmetric, three cases can be studied for this immunity analysis. In the first case, when two nodes are inside of the LSEDUT, there are different analysis for the two pairs of nodes inside of LSEDUT [25], which yields three cases: 1a, 1b, and 1c.

Case 1a: if these pairs of nodes are inside of the LSEDUT and the triple-level CG-SIM is not affected by DNU. There are six key pairs of LSEDUT nodes [25]. These pairs are <N1, N2>, <N3, N4>, <N5, N6>, <N7, N8>, <N9,N10>, and <N11, N12>, which have the same situation against DNU. The explanation of their immunity is as follows. When D 0, N2, N4, N6, N8, N12 are set on the low logic state and all of the PMOSs of the 2-input C-elements are turned ON, and, N1, N3, N5, N7, N9, and N11 are set to high logic state: if N1 and N2 are affected (N1 is discharged to 0 and N2 is charged to 1), n24 and p2 transistors are turned off and transistors p3, n2, n5 are turned ON. Since n6 is off, N3 cannot discharge through n5 to the ground. So other nodes in the LSEDUT except N1, and N2 are not affected by DNU, then N1, and N2 self-recover from N12 and N3, respectively. This shows immunity of the proposed D-latch against DNU in case 1a.

Case 1b: in this case, the pairs inside the LSEDUT to be considered are (1) <N1, N4>, <N3, N6>, <N5, N8>,<N7, N10>, <N9, N12>; (2) <N2, N3>, <N4, N5>, <N6, N7>, <N8, N9>, <N10, N11>, <N12, N1>; (3) <N2, N5>, <N4, N7>, <N6, N9>, <N8, N11>, <N10, N1>,and <N12, N3>. When D 0, N4 0 and N1 1, if, for example, N1 and N4 are affected, N1 will become 0 and N4 will become 1, and n24, p6, and p9 will be turned off and p3, n6, and n9 will be turned ON. Since p3 is ON, N2 is unstable but N5 cannot discharge because n10 is turned off and there isn't any path through n9 to the ground. Although N2 is unstable, it cannot turn to high logic level by any SNU. N4 and N1 are self-recovered by N5 and N12, respectively. Even, if N2 is affected by SNU, it becomes high logic level, N2 and N4 can upset N3, which means that N2 and N4 cannot be self-recovered; however, this upset cannot change the value of N16 because N14 isn't affected. This shows immunity of the proposed D-latch against DNU in case 1b.

Case 1c: in this case, the two pairs affected are inside the LSEDUT including (1) <N1, N3>, <N3, N5>, <N5, N7>,<N7, N9>, <N9, N11>, <N11, N1> (2) <N2, N4>, <N4, N6>, <N6, N8>, <N8, N10>, <N10, N12>. If N1 and N3 are affected, for D 0, N2 0, and N1.1 and after charge injected to N1 and N3, N1 and N3 are discharged to ''0'', n24 and n4 are turned off and p3 and p7 are turned ON. This situation makes N2 to turn to the high logic level and n4 becomes unstable which means that N2 and N4 cannot be self-recovered. In spite of that, this soft error can be filtered by the triple-level CG-SIM and it will not appear at Q which means the proposed D-latch is immune against DNU in case 1c.

Case 2: DNU affects one node in the triple-level CG-SIM and one node of LSEDUTs. This situation for LSEDUTs and the triple-level CG-SIM is the same since they are affected by SNU. As the structure of the proposed D-latch is symmetric, the pairs that should be considered are <N1, N13>, <N1, N16>, and <N1, Q>. In this situation, as explained before if N1 is upset, N3 will not be affected and the LSEDUT is self-recovered from SNU; therefore, SNU in N1 cannot change the value of N13. Even if there is a SNU in N13 simultaneously, as N14 is not affected by any DNU, N16 will not be affected and it would have the valid value, therefore Q will store its valid data. Also, other pairs of nodes in case 2 have the same analysis, which means that Q is immune against DNU in this case, therefore, this proposed D-latch is immune against DNU in case 2.

Conclusion

The proposed D-latch has an additional feature with regard to the recently proposed QNUTL-CG D-latch (able to tolerate QNUs): it can mask SET in the input signal, without impacting on the power consumption (as compared with the QNUTL-CG D-latch). This lower power consumption with the extra SET masking feature and better process variation reliability is achieved by using clock-gating technology.

Future Enhancement

The integration of multiple functions into a single chip can help to reduce the overall size and power consumption of a system. Future enhancements to the design could focus on integrating additional functionality, such as memory or arithmetic logic units, into the same chip.Although the current design is highly reliable, there is always room for improvement. Future enhancements could focus on improving the resistance of the D-latch to other types of radiation, such as cosmic rays or electromagnetic interference.

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