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Design Of Low Power Double Edge Triggered Flip-Flop Circuit

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Abstract ***In this paper, we compare three previously published static double edge-triggered (DET) flip-flops with a proposed design for their transistor counts and power consumptions. The proposed DET flip-flop uses only 12 transistors in addition to the clock driver, and hence requires a small area. Several HSPICE simulations with different input sequences show that the proposed DET flip-flop reduces power consumption up to 85%, as compared to conventional DET flip-flops. A new technique for pulse generation circuit of dual edge triggered flip flop for low power is presented in this paper which enables the flip flop to be operated at 1.2 V. By incorporating a new fast latch and employing conditional pre-charging, dual edge triggered flip flop is capable of achieving low power consumption that has smaller delay. According to simulation on Spectre simulator, it has been observed that total power consumption of proposed flip flop at 0.67 switching activity is 30.16% and 27.36% less than that of previous arts DSPFF and SCDFF respectively. Clock-gated sense-amplifier is incorporated to reduce power consumption at low switching activity. Proposed flip-flop is capable to reduce Clock to output delay up to 44% of that of DSPFF.***

1. INTRODUCTION

In the past, the major concerns of the very large scale integrated (VLSI) engineers were area, performance, cost and reliability; power considerations were mostly of only secondary importance. Currently, several VLSI implementations are described in CMOS technology. Power consumption of VLSI chips is becoming an increasingly critical problem as modern VLSI circuits continue to grow and technologies evolve. In portable systems, very low power consumption is desired in order to increase battery life. In order to reduce the complexity of circuit design, a large proportion of digital circuits are synchronous circuits; that is, they operate based on a clock signal. Among the more popular synchronous digital circuits are edge-triggered flip-flops. The total clock related power consumption in synchronous VLSI circuits can be divided into three major factors: power consumption in the clock network, power consumption in the clock buffers, and power consumption in the flip-flops. Therefore, the improvement of such flip-flops circuits a decreasing in power consumption, without impairing other characteristics, is of prime importance to the VLSI industry.
Edge-triggered flip-flops are often used in computational circuits to operate in selected sequences during recurring clock intervals to sample and hold data for a limited time period sufficient for other circuits within a system to further process data. Edge-triggered flip-flop circuits may be classified into one of two types. The first type latches data on either the rising edge or falling edge of a clock pulse, that is, these so-called single edge-triggered (SET) flip-flops typically latch data either on the rising or the falling edge of the clock cycle. Latches typically form the master or slave half of an edge-triggered flip-flop, or both. Thus, a flip-flop is often constructed from a master latch and a slave latch, in which the output of the master latch is the input of the slave latch, and the output of the slave latch provides the output of the flip-flop. A conventional SET flip-flop is triggered either at the rising edge or the falling edge of a clock cycle. Referring to FIG. 1, it illustrates the circuit structure of a typical conventional rising edge trigger flip-flop.

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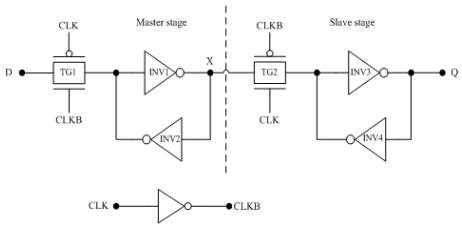

Fig. 1 The conventional SET flip-flop

The master stage has a conventional transmission gate (TG1) to receive a data signal D. As is well known, TG1 is controlled to transmit the received data signal D by the true and complementary clock signals CLK and CLKB respectively. Thus, TG1 is controlled to pass the data signal D prior to a rising edge. The slave stage also includes a transmission gate TG2 and a latch. However, TG2 is configured to be conductive when TG1 is non-conductive and vice versa. Therefore, the conventional rising SET flip-flop is capable of performing one bit access during a clock cycle. However, the operation is merely performed at the rising edge of a clock and cannot be performed at the falling edge of the clock. These arrangements are inefficient as half of the clock edges are wasted, data flow tends to be slow, i.e., at only one half the clock edge frequency. Also, because of their single clock-edge operation, SET flip-flops incur the power cost of operating at two clock edges per interval while using only one of the edges.

Proposed Double Edge-Triggered Flip-Flop

The proposed DET flip-flop is illustrated in FIG. 6. This design can be thought of as a parallel connection of two latches, one transparent when the clock is high and the other transparent when the clock is low, with a multiplexor selecting the output of the latch that is in hold state. In the upper data path, transistor MP2 provides feedback to pull up storage node X substantially to VDD when signal node XB is low. Pull-up transistor MP2 ensures that, although a clock signal applied to the gate of MN1 does not reach the voltage VDD, the storage node X can still reach VDD. In the lower data path, transistor MN2 provides feedback to pull down node Y to a lower voltage when the signal node YB is high. The inclusion of pull-down transistor MN2 ensures that, although the clock signal applied to the gate of MP1 does not reach the voltage GND, the storage node Y can still reach GND.

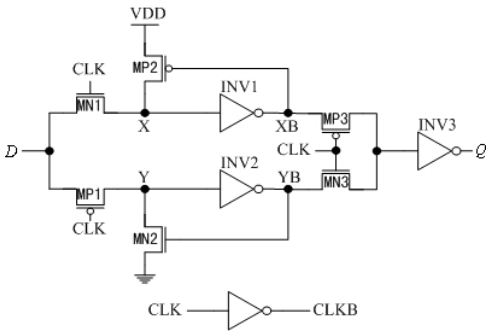

Fig.11 The proposed DET flip-flop

When the clock is in the "high" state, for the upper data path, the input signal D is quickly conducted into the node XB. If the input signal D is "high", node X goes to the logic high with help from the pull-up transistor MP2. Node X remains high as long as input signal D is at the high level. Meanwhile, for the lower data path, the previously hold data is quickly pass to the output node Q with help from the transistor MN3. On the contrary, when input signal D falls while the clock is in the "low" state, for the lower data path, the input signal D is quickly conducted into the node YB and node Y goes to the logic low with help from the pull-down transistor MN2. Node Y remains low as long as input signal D is at the low level. Meanwhile, for the upper data path, the previously hold data is quickly pass to the output node Q with help from the transistor MP3.

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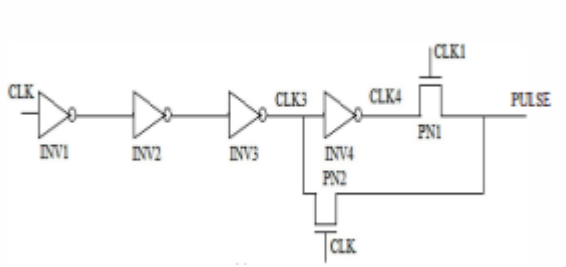

Fig 12: Dual edge triggered static pulsed flip-flop (DSPFF): (a) Pulse generator

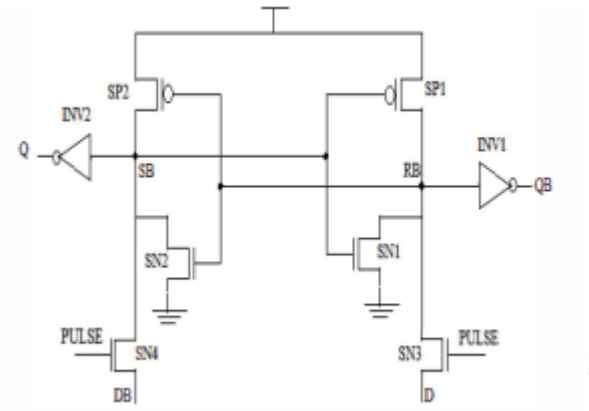

Fig 12: Dual edge triggered static pulsed flip-flop (DSPFF): (b) Static latch.

In this section, a new dual edge triggered flip-flop is proposed. This flip-flop consists of pulse generator, sense amplifier, and latch. The schematic diagram of proposed flipflop is shown in fig. 3. A new scheme is used for generation of pulse which generates undistorted pulse at high frequency and low operating voltage. This circuit avoids series of inverters to generate delayed versions of clock thus avoids charging and discharging of clocks output nodes. Thus a lot power is saved and circuit operates at low power comparatively. At both positive as well as negative edges of clock, pulse node gets charged through negative pulse controlled transistors and after some delay, it starts to discharge through transistor PNI. Delay depends on the processing time of transistors of buffer used in feedback path. Appropriate delay can set by adjusting aspect ratios of buffers' transistors. The pulse generator circuit can be shared by multiple flip-flops when a group of flip-flops are located closely. In sense amplifier, conditional pre-charge technique is used to simplify the discharge path of intermediate nodes SB and RB. Two input controlled pMOS transistors are used to charge SB and RB nodes.

Simulation And Results

To evaluate performance, different flip-flop structures discussed in this paper was designed using a 0.18 um CMOS technology. All simulations are carried out at nominal conditions: VDD=1.8V and at room temperature. The simulated waveform of the proposed DET flip-flop .As the power consumption is related to the data sequence, in the following simulations we adopted two different data sequences to compare the power consumption of these flip-flop structures discussed in this paper. The first data sequence is 101010, and the second data sequence is 11001100. For the edge-triggered flip-flops in Table 1, a comparison among

different parameters, only for the data sequence is 11001100, for a data rate of 1000 Mbits/sec and the output load of 0.5pF is presented. The parameters include the total number of transistors, the delay from data to the output (D-Q), the total power consumption, and the power-delay product (PDP). As shown in the Table, the number of transistors in this work is the same as SET structure and is less than other structures. Compared to SET flip-flop, the power consumption of this work is 78.06% less while the power-delay product of this work is 83.43% less, respectively.

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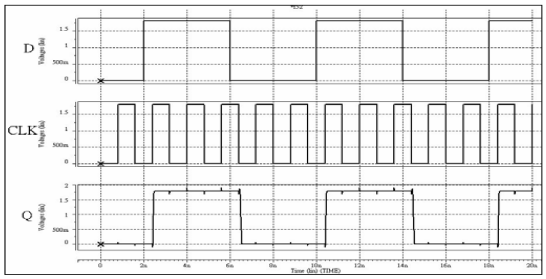

Fig.14 Transient analysis waveforms of this work

TABLE 1: Comparison among various structures discussed in this paper

FF	# of transistors	D-Q (pS)	Power (uW)	PDP (fJ)
Fig. 1	12	139	266.32	370.18
Fig. 2	16	151	402.21	607.34
Fig. 3	14	200	273.90	547.80
Fig. 4	16	176	230.50	405.68
Fig. 5	18	270	260.27	702.73
This work	12	105	58.42	61.34

Next, we compare three previously published static double DET flip-flops with the proposed design for their power consumptions. From Table 2 and Table 3, one finds that the proposed circuit which is composed by 12 transistors always consumes less power than Hossain et al.'s circuit under varying data rates. For the proposed circuit, the saving power percentage is between 72% and 88% for input data sequence 101010, and the saving power is between 80% and 85% for input data sequence 11001100.

TABLE 2: Input Data Sequence is 101010 (the percentage is related to Fig. 2)

Data Rate (Mbits/s)	Fig. 2 (uW)	Fig. 3 (uW)	Fig. 5 (uW)	Fig. 6 (uW)
2000	1061.8	389.62 (-63.31%)	533.09 (-49.79%)	194.61 (-81.67%)
1667	601.98	368.48 (-38.79%)	494.63 (-17.83%)	163.48 (-72.84%)
1333	495.13	299.58 (-39.49%)	415.10 (-16.16%)	127.08 (-74.33%)
1000	388.69	221.88 (-42.92%)	384.37 (-0.01%)	97.57 (-74.90%)
667	388.26	153.96 (-60.35%)	296.06 (-23.75%)	66.10 (-82.98%)
333	228.25	75.84 (-66.77%)	218.07 (-4.46%)	30.70 (-86.55%)
167	131.84	[illegible] (-69.43%)	178.12 (35.10%)	15.36 (-88.35%)

Fig. 8 is curve for Table 2 and Table 3. From this figure, one finds that the proposed circuit always consumes less power than the others under varying data rates. And, the Pedram et al.'s flip-flop consumes more power than the circuit of the other flip-flops by influence of charge sharing.

Conclusion

The proposed circuit only uses 12 transistors, which is less transistors than in any current DET flip-flop construction. To compare with the SET flip-flop shown in Fig. 1, the proposed circuit has two less transistors. In addition, the proposed circuit consumes less power than the others under varying data rates. Hence, for a high data rate, the proposed flip-flop is more suitable for low power circuit application than the existing flip-flops. This paper presents a novel design for dual edge triggered flip-flop for low power and high-performance applications. DET-SAFF achieves low power by incorporating dual edge triggering technique and conditional pre-charging. It also improves latency by using fast latch. Proposed flip-flop has low latency which provides some attributes like robustness and design flexibility. DET-SAFF can be used in critical path because of less latency and low power consumption at low switching activity.

Future Enhancement

As emerging technologies such as quantum computing and neuromorphic computing become more prevalent, integrating low-power DETFFs with these technologies can lead to improved energy efficiency and performance.
Developing tools for automated design of low-power DETFFs can enable faster and more efficient circuit design.

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