IJIRMET
ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering and Technology
Vol. 8, Issue 6, June 2023

Analysis Of Passive Charge Sharing – Based Segmented Sar Adcs

[1] Priya E,[2] Mr.P.Boopathi

[1] M.E VLSI PG Student, Thirumalai Engineering College, Kanchipuram, India

[2] M.E Assistant Professor, Dept. of ECE, Thirumalai Engineering CollegeKanchipuram,India.

Abstract *This article presents the theoretical analysis of pas- sive charge sharing-based segmented successive-approximation- register (SAR) analog-to-digital converter (ADC), where the pre- cise reference source in a capacitive digital-to-analog converter (CDAC) is replaced by a capacitor that is β times larger than its bit capacitor and precharged to the reference level, known as a reference charge reservoir (RCR). A segmented SAR-ADC uses a coarse SAR-ADC to compute some most significant bits (MSBs). Four methods, namely aligned switching (AS) with bitwise RCRs, AS with a subsample-wise RCR, detect-and-skip aligned switch- ing (DAS-AS) with bitwise RCRs, and DAS-AS with a subsample- wise RCR are introduced for setting fine MSBs. Closed-form analytic expressions of the reference error due to the finite reference capacitance are derived and validated by behavioral modeling and circuit simulation of an 11-bit 50 MS/s segmented SAR ADC in 65-nm CMOS technology. The error expressions can be used to select one of the four methods for setting the fine MSBs and to determine β for the required linearity or for implementing digital circuitry for precise error correction.*

Index Terms *— Bitwise reference charge reservoirs (RCRs), reference-buffer free, segmented architecture, subsample-wise reference charge reservoir (RCR), successive-approximation- register (SAR) ADC..*

1. INTRODUCTION

Successive approximation register (SAR) analog-to- digital converters (ADCs) are the most energy-efficient data conversion solutions for 10–100-MHz sampling rates with 10–12 bit resolution [1]–[4]. Combined with pipeline [5], [6], time interleaving [6], and noise shaping [7], SAR ADCs are being extended to applications with even higher speed up to GHz [8] or higher resolution up to 18 bits [9].One major reason why the SAR-ADC architecture is increasingly popular is its scalability with the process technology and its amenability to a digital-centric design methodology. To remove power-hungry buffers associated with precise capacitive digital-to-analog converter (CDAC) refer- ences, various forms of passive charge sharing have been introduced [10]–[16]. In particular, a Sample-wise Switched Reference Charge Reservoir (SS-RCR) technique was intro- duced [12], where a sufficiently large capacitor (reservoir), β times larger than the total bit capacitors, precharged to the reference voltage level during the sample phase acts as the reference for all bit switchings during the entire ADC. Very recently, a Bitwise Switched Reference Charge Reservoir (BS- RCR) technique was proposed [13], where the charge reservoir capacitor is split into the corresponding bit, and before each bit switching, the corresponding bit charge reservoir capacitor is precharged to the reference levels and used as the reference during each bit decision. With BS-RCRs, a 16-bit 1 MS/s SAR-ADC in 55 nm CMOS with 6.95 mW with a FoM of 738 fJ/conversion-step [14] and a 16-bit 16 MS/s SAR in 55 nm CMOS with FoM 157.4 fJ/conversion-step [15] have been demonstrated. It has been approved theoretically [16] that the BS-RCR technique yields better linearity than the SS-RCR technique, a seemingly counterintuitive fact. Further- more, the reference error due to finite BS-RCRs appears in the form of digitally correctable bit weight error, where the i th bit weight is attenuated by $12^{i+1-N}\beta$ for an N -bit SAR-ADC. To reduce the energy associated with most significant bit (MSB) switching, a dominating factor in affecting SAR-ADC switching energy efficiency, a segmented architecture has been developed, where a coarse SAR-ADC computes the MSBs for a fine SAR-ADC [17]. This article extends reference charge reservoirs (RCRs) to segmented SAR-ADC design. Since BS-RCR has better linearity, we use it for the coarse ADC, as well as fine ADC LSB switching. For copying the results from coarse ADC to the MSBs of the fine ADC, there are two switching methods: aligned switching (AS), all bits are switched together; detect-and-skip AS (DAS-AS) [17], where only some bits are switched. For the fine MSBs reference, it can be bitwise RCRs and subsample-wise RCR. This leads to four switching methods for setting fine MSBs, known as AS with bitwise RCRs, AS with a subsample- wise RCR, DAS-AS with bitwise RCRs, and DAS-AS with a subsample-wise RCR.Theoretically, we have derived the analytical formula of the reference error for various RCR-based segmented SAR- ADC switching schemes. From these formulae, we have proved that successive decisions using bitwise RCRs and fine MSB switching using DAS-AS subsample-wise RCR yields the near the smallest reference error while saving most switching energy.

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, June 2023

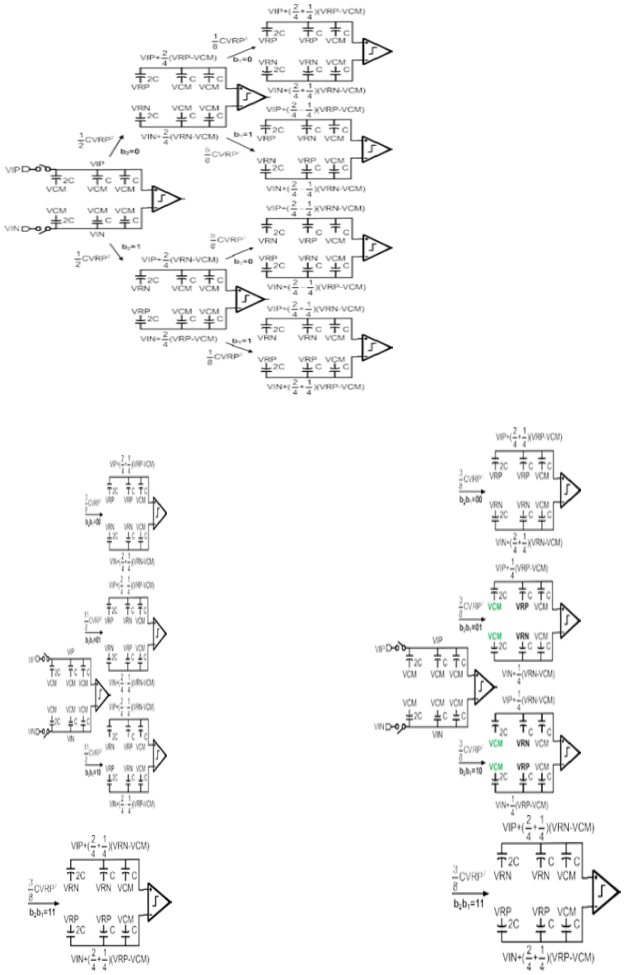


Fig. 1. Three bit charge redistribution CDAC switching examples. (a) MCS. (b) AS. (c) DAS-AS
ADCs. Section III presents the theoretical analysis of the RCR-based segmented SAR-ADCs. Simulation validation and discussion are described in Section IV.

Existing Method

Converter Architectures

An overwhelming variety of ADCs exist on the market today, with differing resolutions, bandwidths, accuracies, architectures, packaging, power requirements, and temperature ranges, as well as hosts of specifications, covering a broad range of performance needs. And indeed,there exists a variety of applications in data-acquisition, communications, instrumentation, and interfacing for signal processing, all having a host of differing requirements.Considering architectures, for some applications just about any architecture could work well; for others, there is a "best choice". In some cases the choice is simple because there is a clear-cut advantage to using one architecture over another. For example, pipelined converters are most popular for applications requiring a throughput rate of more than 5 MSPS with good resolution. Sigma-delta converters are usually the best choice when very high resolution (20 bits or more) is needed. But in some cases the choice is more subtle. For example, the sigma-delta AD7722 and the successive- approximations AD974 have similar resolution

(16 bits) and throughput performance (200 ksps). Yet the differences in their underlying architectures make one or the other a better choice, depending on the application.The most popular ADC architectures available today are successive approximations (sometimes

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, June 2023

called SAR because a successive-approximations (shift) register is the key defining element), flash (all decisions made simultaneously), pipelined (with multiple flash stages), and sigma-delta (SD), a charge- balancing type. All A/D converters require one or more steps involving comparison of an input signal with a reference. Figure 1 shows qualitatively how flash, pipelined, and SAR architectures differ with respect to the number of comparators used vs. the number of comparison cycles needed to perform a conversion

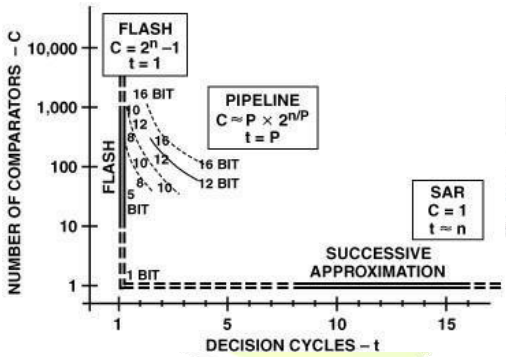


Figure 1. Tradeoff between decision cycles and comparators.

Simulation Validation And Discussion

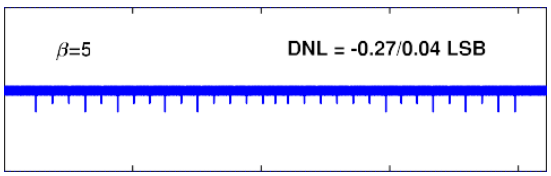
Behavioral modeling and schematic level simulations were performed to validate the analysis of the segmented SAR ADCs with RCRs. The simulated segmented SAR ADCs with RCRs is shown in Fig. 5, and is implemented in a 65 nm CMOS technology. The coarse unit capacitance Cc is 2 fF whereas the fine unit capacitance CF is 1 fF.

Static Performance of RCR-Based Segmented SAR ADC

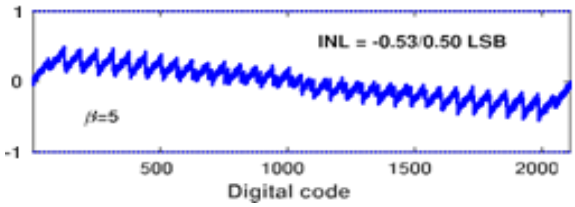
Using analytic formula derived, we can compute, simulate, and compare the static performance differential nonlinearity (DNL) and integral nonlinearity (INL) of RCR-based seg- mented SAR ADCs. Fig. 14(a)–(d) upper four plots show the respective DNLs and INLs of a segmented 11-bit SAR ADC with a 5-bit coarse and a 12-bit fine SAR ADC using four switching methods for the fine MSBs and $\beta = 5$. With $\beta = 5$, the 5-bit coarse ADC can compute output digits correctly. These five digits are loaded to the 5-bit fine MSBs using one of four switching methods. As we can see, AS with bitwise RCRs in Fig. 14(a) yields the best static performance (INL/DNL less than 0.5 LSB). In fact from (7), we can compute the reference error for the 5-bit fine MSBs with $\beta = 5$ as $1 - \alpha(M)$ $(VRP - VRN) \approx 0.006(VRP - VRN)$ $1 < 27$ $(VRP - VRN)$. (28)

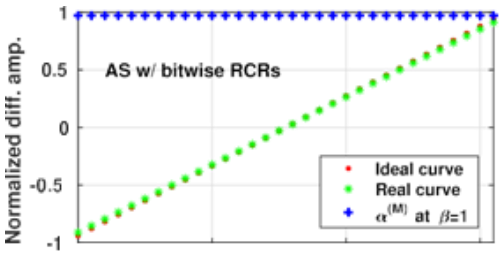
Thus, the 7-bit fine LSBs can compute results correctly. This yields the INL to be in the range of 0.5 LSB.The DNLs and INLs in Fig. 14(b)–(d) have some simi- larities. The segmented misaligned ADC transfer curves lead to different analog input mappings to the same digits, thus causing the DNL at the digits corresponding to misaligned transfer curves to be more than 1 LSB. The INL is the deviation in LSB of the actual transfer function of the ADC from the ideal transfer curve ($\beta =$). The linearity of the segmented ADC is mainly decided by the reference error introduced in the 5-bit fine MSBs. This can be seen from $\alpha(M)$, input-normalized ideal and actual transfer curves of 5-bit fine MSBs versus coarse digits plotted in Fig. 14(a)–(d) for four cases. The factor $\alpha(M)$ affects the transfer curve through modulating the reference voltage in a manner of $\alpha(M)(VRP - VRN)$. Thus, the larger $\alpha(M)$, the smaller the reference error $1 - \alpha(M)$, the modulated actual transfer curve is more close to the ideal curve. To have a better visualization of reference modulation, β 1 is used in plotting $\alpha(M)$ and actual transfer curves. We see that the deviation of the actual transfer curve from the ideal curve in the 5-bit MSBs has the same shape with the INL of the 11-bit segmented SAR ADC. To minimize the reference error, $\alpha(M)$ shall be as large as possible. While for minimum switching energy associated with the MSBs switching, DAS-AS with a subsample-wise RCR is a good option.

A)

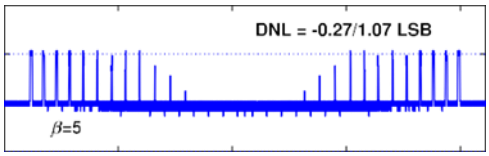


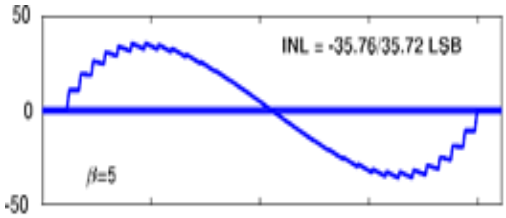
ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, June 2023

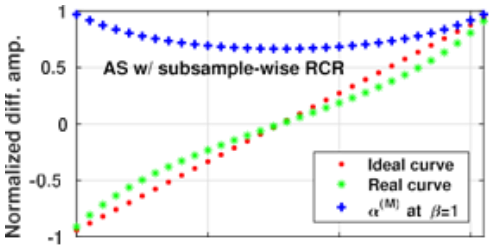




B)







Conclusion

This article presented the theoretical analysis of an RCR technique for segmented SAR-ADC design. Theoretical analy- sis and simulation have been performed to analyze the error due to the finite reference capacitance. Both the analysis and simulation show that in a segmented SAR ADC, successive bit decisions in both coarse and fine SAR ADCs using bitwise RCRs and the MSB copy from the coarse ADC to the fine ADC using AS with bitwise RCRs, can reduce β significantly compared with other cases without any performance loss.While the fine MSB copy using detect-and-skip, AS with subsample-wise RCR can reduce reference error and switching energy compared with a successive decision only SAR ADCs with bitwise or sample-wise RCR that have the same β.

References

1)C. Qi, L. Xiao, J. Guo, and T. Wang, ‘‘Low cost and highly reliable radiation hardened latch design in 65 nm CMOS technology,’’ Microelectron. Rel., vol. 55, no. 6, pp. 863–872, May 2015.
2)H. Wang, X. Dai, Y. Wang, I. Nofal, L. Cai, Z. Shen, W. Sun, J. Bi, B. Li, G. Guo, L. Chen, and S. Baeg, ‘‘A single event upset tolerant latch design,’’ Microelectron. Rel., vols. 88–90, pp. 909–913, Sep. 2018.
3)H. Li, L. Xiao, J. Li, and C. Qi, ‘‘High robust and cost effective double node upset tolerant latch design for nanoscale CMOS technology,’’ Microelectron. Rel., vol. 93, pp. 89–97, Feb. 2019.
4)N. Eftaxiopoulos, N. Axelos, and K. Pekmestzi, ‘‘DIRT latch: A novel low cost double node upset tolerant latch,’’ Microelectron. Rel., vol. 68, pp. 57–68, Jan. 2017.
5)A. Watkins and S. Tragouodas, ‘‘A highly robust double node upset tolerant latch,’’ in Proc. IEEE Int. Symp. Defect Fault Tolerance VLSI Nanotechnol. Syst. (DFT), Sep. 2016, pp. 15–20.
6)C. I. Kumar and B. Anand, ‘‘A highly reliable and energy-efficient triplenode- upset-tolerant latch design,’’ IEEE Trans. Nucl. Sci., vol. 66, no. 10, pp. 2196–2206, Oct. 2019.
7)A. Yan, Z. Xu, X. Feng, J. Cui, Z. Chen, T. Ni, Z. Huang, P. Girard, and X. Wen, ‘‘Novel quadruple-node-upset-tolerant latch designs with optimized overhead for reliable computing in harsh radiation environments,’’ IEEE Trans. Emerg. Topics Comput., vol. 10, no. 1, pp. 404–413, Jan. 2022.
8)A. Watkins and S. Tragoudas, ‘‘Radiation hardened latch designs for double and triple node upsets,’’ IEEE Trans. Emerg. Topics Comput., vol. 8, no. 3, pp. 616–626, Jul./Sep. 2017.
9)C. Peng, ‘‘Radiation-hardened 14T SRAM bitcell with speed and power optimized for space application,’’ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 27, no. 2, pp. 407–415, Nov. 2019.
10)Y.-C. Chien and J.-S. Wang, ‘‘A 0.2 V 32-Kb 10T SRAM with 41 nW standby power for IoT applications,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 65, no. 8, pp. 2443–2454, Aug. 2018.
11)Y. Li, H. Cai, and C. Xiaowen, ‘‘Impact of adjacent transistors on the SEU sensitivity of DICE flip-flop,’’ IEICE Electron. Exp., vol. 14, no. 5, pp. 1–8, 2017.
12)R. Song, J. Shao, B. Liang, Y. Chi, and J. Chen, ‘‘MSIFF: A radiationhardened flip-flop via interleaving master-slave stage layout topology,’’ IEICE Electron. Exp., vol. 17, no. 4, pp. 1–5, 2020.
13)J. Jiang, Y. Xu, J. Ren, W. Zhu, D. Lin, J. Xiao, W. Kong, and S. Zou, ‘‘Low- cost single event double-upset tolerant latch design,’’ Electron. Lett., vol. 54, no. 9, pp. 554–556, May 2018.
14)T. Calin, M. Nicolaidis, and R. Velazco, ‘‘Upset hardened memory design for submicron CMOS technology,’’ IEEE Trans. Nucl. Sci., vol. 43, no. 6, pp. 2874– 2878, Dec. 1996.
15)A. Yan, Z. Huang, X. Fang, Y. Ouyang, and H. Deng, ‘‘Single event doubleupset fully immune and transient pulse filterable latch design for nanoscale CMOS,’’ Microelectron. J., vol. 61, pp. 43–50, Mar. 2017.
16)Z. Huang, H. Liang, and S. Hellebrand, ‘‘A high performance SEU tolerant latch,’’ J. Electro. Test., vol. 31, no. 4, pp. 349–359, Jul. 2015.
17)A. Yan, Y. Ling, J. Cui, Z. Chen, Z. Huang, J. Song, P. Girard, and X. Wen, ‘‘Quadruple cross-coupled dual-interlocked-storage-cells-based multiple-node-upset- tolerant latch designs,’’ IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 67, no. 3, pp. 879–890, Mar. 2020.