ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering and Technology
Vol. 8, Issue 6, March 2024

An Ultra-Low-Power Track and-Hold Amplifier

[1] A.Sonia,[2] E.C.Anjaneyan

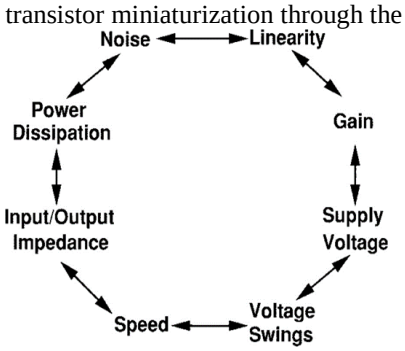
[1] M.E VLSI, Dept of ECE, Thirumalai Engineering College, Kanchipuram

[2] Dept of ECE, Thirumalai Engineering College, Kanchipuram.

Abstract *The future of electronics is the Internet of Things (IoT) paradigm, where "always-on" devices and sensors monitor and transform everyday life. A plethora of applications (such as navigating drivers past road hazards or monitoring bridge and building stresses) employ this technology. These unattended ground-sensor applications require decade(s)- long operational lifetimes without battery changes. Such electronics demand stringent performance specifications with only nano-Watt power levels. This thesis presents an ultra-low-power track-and-hold amplifier for such systems. It serves as the front-end of a SAR-ADC or the building block for equalizers or filters. This amplifier's design attains exceptional hold times by mitigating switch subthreshold leakage and bulk leakage. Its novel transmission-gate topology achieves wide-swing performance. Though only consuming 100 pico-Watts, it achieves a precision of 7.6 effective number of bits (ENOB). The track-and-hold amplifier was designed in 130-nm CMOS..*

1. INTRODUCTION

Modern electronics emphasize portability and long battery-life. Customers no longer tether themselves to power outlets. Satellite phones communicate from anywhere on earth. Smart phones blur distinctions between personal computing and telecommunication. Remote sensors reduce threats from natural forces. RFID1 tracking revolutionizes inventory management. Medical diagnosis through ingestible electronic devices extend lives. These and similar battery-operated applications are ubiquitous today. What enables these advances? Not the batteries themselves. Chemical-energy density in batteries improves slowly (at about 3% per year over the past 60 years) [1]. Market demands compel creative circuit designers to seek less power-hungry designs for these electronic devices. Researchers have explored ultra-low-power circuit design. In the 1960s and 1970s, Swiss watchmakers pioneered subthreshold operation for analog and digital CMOS circuits [2][3]. When operated below their thresholds, CMOS transistors (generally considered majoritycarrier devices) become minority-carrier devices. Circuit operation continues, but only draws a trickle of charge. Further, transistor miniaturization through the decades gave designers more flexibility, enabling previously unattainable applications



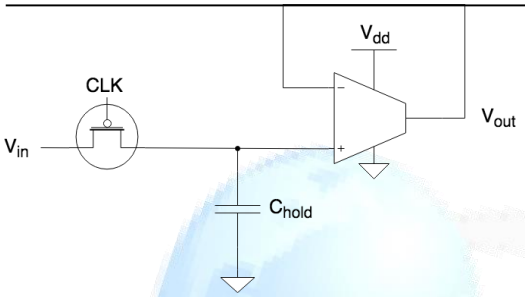
Analog Design Octagon [5]

Proposed System

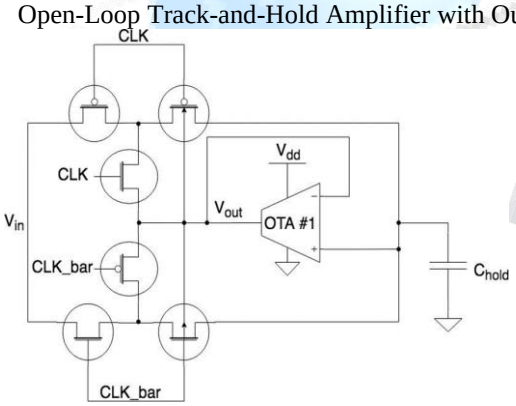
Open-Loop Track and Proposed system

Open-Loop Track-and-Hold Amplifier Topology The previous chapter concluded that the open-loop track-and-hold amplifier topology is optimal for ultra-low-power design. However, ensuing performance issues abound. This section will develop an improved circuit to reduce subthreshold leakage effects, bulk leakage, and non-linear conductance. An output buffer to the original open-loop track-and-hold amplifier

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, March 2023



Open-Loop Track-and-Hold Amplifier with Output Buffer



Wide-Swing Open-Loop Topology

For most of the range. The full brunt of charge injection appear only at the extrema. This"uncertainty" may be detrimental and may demonstrate a hysteresis effect in the circuit.

Walden Figure of Merit (FOM)

While designing this track-and-hold amplifier, no comparable track-and-hold amplifiers appear in the literature. Yet, determining the circuit's efficacy requires comparing it to other designs. The track-and-hold/sample-and-hold amplifier is the typical first stage in an ADC. The Walden Figure of Merit (FOM) [42] evaluates ADCs:

FOM=Power W/ fsampling2ENOBHz—(4.7)

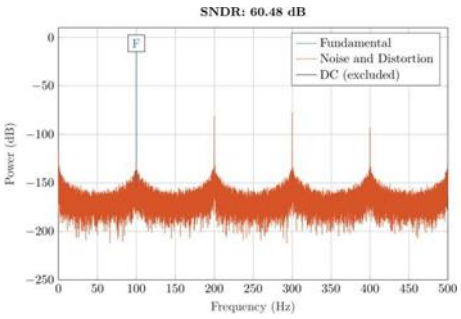
Like ADCs, track-and-hold amplifiers focus on: 1) power, 2) speed (maximum sampling frequency), and 3) precision (ENOB).As the introduction discussed, these specifications trade with each other. For example, doubling the sampling frequency generally requires twice the power consumption. Fortunately, the Walden FOM normalizes these trade-offs, allowing comparison of disparate designs side-by-side.The lower the FOM, the better.

Using the maximum Nyquist sampling frequency of 1 kHz and the average ENOB (for 500 mV input voltage) of 7.58 bits, this thesis' topology achieves:

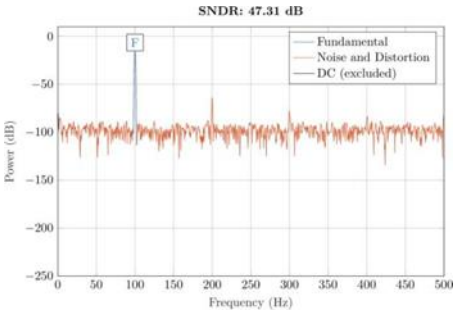
FOM=104.48× 10−12 fW/1×103×27.58HZ—(4.8)

The wide-swing track-and-hold amplifier achieves the best efficiency of all topologies surveyed (see Table 4.3). It improves upon the previous design this author tested [37]. It advances significantly over other designs presented in the literature

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, March 2023



a)Simulation SNDR



b)Experimental SNDR

SNDR for Simulation and Experimentation

Test #	SNDR (dB)	SFDR (dB)	SNR (dB)
	700 mV Peak-to-Peak Amplitude		
Worst	41.91	43.17	46.35
Mean	42.98	45.32	52.52
Best	43.99	47.19	54.11
	500 mV Peak-to-Peak Amplitude		
Worst	46.50	48.89	50.10
Mean	47.37	50.07	51.33
Best	48.04	51.14	53.54

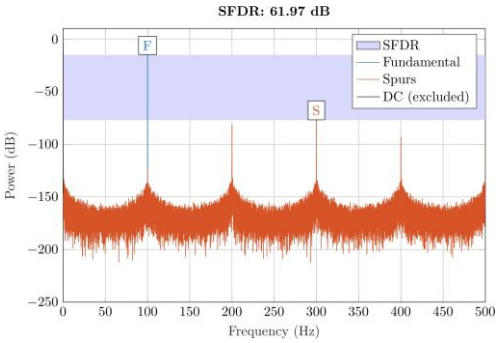
Table 4.2: Worst, Mean, and Best Dynamic

Specs

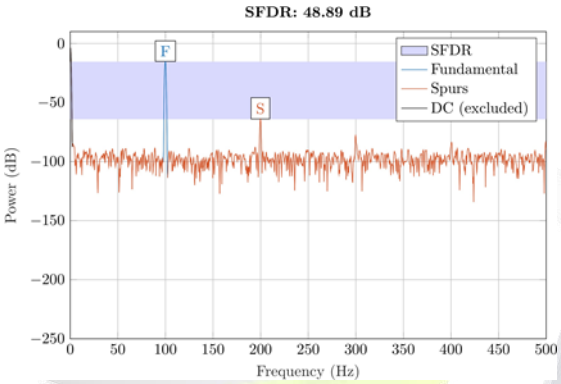
a)Simulation SFDR

a)Simulation SFDR

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, March 2023



a)Simulation SFDR



b)Experimental SFDR

SFDR for Simulation and Experimentation

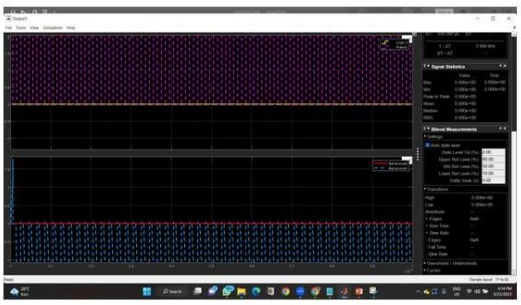
Conclusion

This topology achieves many of the specifications set forth in Chapter 3 (Table 5.1 compares targeted and achieved specifications). Particularly, its power efficiency (Walden FOM)1 exceeds that found in the literature for competing topologies. It would be an excellent front-end for an ultra-low-power, 8-bit, SAR-ADC. Unattended ground sensors (requiring decades-long battery lifetimes) could employ such an ADC. Otheruses are battery-operated bio-potential applications (with ultra-low signal frequencies). Thistrack-and-hold amplifier stems leakage paths, so it enhances integrity of very-low-frequency signals. It can also be a building block for an ultra-low-power equalizer or analog FIR filter. It can enhance the signal integrity of low-frequency communications circuits.

Future Work

This author will re-fabricate this circuit as part of an ultra-low-power analog tapped-delay-line. This will enable testing an improved version in a system. Circuit improvements willprecede incorporating it into that design. The design process and experimental testing surfaced a few circuit improvements. First, a higher-gain OTA would improve voltage offsets and enable working closer to the rails. Second, both OTAs and the on-chip pad driver require a redesign to accept rail-to-rail inputs and produce rail-to-rail outputs. This will enhance the overall circuit's dynamic performance. Third, the holding capacitor size should increase. The circuit surpassed the goals, but the sum of all the offsets became significant. A larger holding capacitor will reduce many circuit imperfections and increase consistency between chips.

RESULTS ANALYSIS



References

1. E. Vittoz, B. Gerber, and F. Leuenberger, "Silicon-gate CMOS frequency divider for electronic wrist watch," IEEE Journal of Solid-State Circuits, vol. 7, no. 2, pp. 100–104, Apr 1972.
2. E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," IEEE Journal of Solid-State Circuits, vol. 12, no. 3, pp. 224–231, Jun 1977.
3. S. Shapero, A. S. Charles, C. J. Rozell, and P. Hasler, "Low Power Sparse Approximation on Reconfigurable Analog Hardware," IEEE Journal on Emerging and Selected Topicsin Circuits and Systems, vol. 2, no. 3, pp. 530–541, Sept 2012. 2
4. B. Razavi, "CMOS technology characterization for analog and RF design," IEEE Journal of Solid-State Circuits, vol. 34, no. 3, pp. 268– 276, Mar 1999. 2
5. P. Harpe, "Successive Approximation Analog-to-Digital Converters: Improving Power Efficiency and Conversion Speed," IEEE Solid-State Circuits Magazine, vol. 8, no. 4, pp. 64–73, Fall 2016. 3, 21
6. S. Kiriaki, et al., "A 160-MHz analog equalizer for magnetic disk read channels," IEEE Journal of Solid-State Circuits, vol. 32, no. 11, pp. 1839– 1850, Nov 1997. 3, 21
7. B. Razavi, Principles of Data Conversion System Design. IEEE Press, 1995. 5, 23
8. B. Razavi, "Design of sample-and-hold amplifiers for high-speed low voltage A/D converters," in Proceedings of CICC 97 - Custom Integrated Circuits Conference, May 1997, pp. 59–66.
9. R. A. Mao, K. R. Keller, and R. W. Ahrons, "Integrated MOS analog delay line," IEEE Journal of Solid-State Circuits, vol. 4, no. 4, pp. 196–201,Aug1969.
10. E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operations," IEEE Journal of Solid-State Circuits, vol. 12, no. 3, pp. 224–231, Jun 1977.
11. R. Baker, CMOS: Circuit Design, Layout, and Simulation, ser. IEEE Press Series on Microelectronic Systems. Wiley, 2011.
12. T. S. Lee, C. C. Lu, and J. T. Zhan, "A 250MHz 20mW 11Bit Low-Hold-Pedestal CMOS Fully Differential Track-and-Hold Circuit," in 2007 IEEE Conference on Electron Devices and Solid-State Circuits, Dec 2007, pp. 889–892. 62
13. H. G. Wei, U. F. Chio, Y. Zhu, S. W. Sin, S. P. U, and R. P. Martins, "A Rapid Power-Switchable Track-and-Hold Amplifier in 90-nm CMOS," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 57, no. 1, pp. 16–20, Jan 2010. 62
14. H. Nyquist, "Certain factors affecting telegraph speed," The Bell System Technical Journal, vol. 3, no. 2, pp. 324–346, April 1924. 76

15. C. E. Shannon, “Communication in the Presence of Noise,” Proceedings of the IRE, vol. 37, no. 1, pp. 10–21, Jan 1949. 76
16. P. R. Gray, Analysis and Design of Analog Integrated Circuits, 5th ed. Wiley Publishing, 2009. 78, 79