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Power Efficient Matrix Vector Multiplication For Mimo System Using Voting Technique

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Abstract: ***In this work, we present an approach to alleviate the potential benefit of adder graph algorithms by solving the transposed form of the problem and then transposing the solution. The key contribution is a systematic way to obtain the transposed realization with a minimum number of cascaded adders subject to the input realization. In this way, wide and low constant matrix multiplication problems, with sum of products as a special case, which are normally exceptionally time consuming to solve using adder graph algorithms, can be solved by first transposing the matrix and then transposing the solution. Examples show that while the relation between the adder depth of the solution to the transposed problem and the original problem is not straightforward, there are many cases where the reduction in adder cost will more than compensate for the potential increase in adder depth and result in implementations with reduced power consumption compared to using sub-expression sharing algorithms, which can both solve the original problem directly in reasonable time and guarantee a minimum adder depth.***

Keywords: Constant matrix multiplication (CMM), Multiple constant multiplication (MCM),Shift-and-add, Sum of products (SOP),Minimum depth expansion algorithm..

1. INTRODUCTION

MIMO stands for Multiple-input multiple-output. While it involves multiple technologies, MIMO can essentially be boiled down to this single principle: a wireless network that allows the transmitting and receiving of more than one data signal simultaneously over the same radio channel, typically using a separate antenna for the transmitting and receiving of each data signal. Standard MIMO networks tend to use two or four antennas to transmit data and the same number to receive it. Massive MIMO, on the other hand, is a MIMO system with an especially high number of antennas. There's no set figure for what constitutes a Massive MIMO set-up, but the description tends to be applied to systems with tens or even hundreds of antennas. For example, Huawei, ZTE, and Facebook have demonstrated Massive MIMO systems with as many as 96 to 128 antennas. Because MIMO systems need to physically pack more antennas into a small area, they require the use of higher frequencies (and hence shorter wavelengths) than current mobile network standards. The advantage of a MIMO network over a regular one is that it can multiply the capacity of a wireless connection without requiring more spectrum. Reports point to considerable capacity improvements, and could potentially yield as much as a 50-fold increase in future. The more antennas the transmitter/receiver is equipped with, the more possible signal paths and the better the performance in terms of data rate and link reliability. A Massive MIMO network will also be more responsive to devices transmitting in higher frequency bands, which will improve coverage. In particular, this will have considerable benefits for obtaining a strong signal indoors. The greater number of antennas in a Massive MIMO network will also make it far more 2 resistant to interference and intentional jamming than current systems that only utilise a handful of antennas.

Existing Methods

Bit Massive Mu-Mimo Precoding In Vlsi

Oscar Castaneda et al propose two nonlinear 1-bit precoding algorithms and corresponding very large-scale integration (VLSI) designs.

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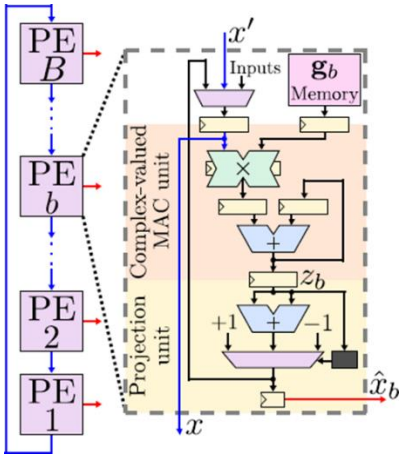
Our algorithms rely on bi-convex relaxation, which enables the design of efficient 1-bit precoding algorithms that achieve superior error-rate performance compared with that of linear precoding algorithms followed by quantization. To showcase the efficacy of our algorithms, we design VLSI architectures that enable efficient 1-bit precoding for massive MU-MIMO systems, in which hundreds of antennas serve tens of user equipments. We present corresponding field programmable gate array (FPGA) reference implementations to demonstrate that 1-bit precoding enables reliable and high-rate downlink data transmission in practical systems.



High-level block diagram of the VLSI architecture for C1PO

The VLSI architecture that implements C1PO as detailed in Algorithm 1 is shown in Figure. Our architecture consists of a linear array of B identical processing elements (PEs) that share a common control unit. The PEs essentially compute the complex-valued matrix-vector product, using a variant of Cannon's algorithm, followed by the projection operation. Each PE b = 1, 2, . . . , B consists of three main building blocks: (i) a gb-memory,(ii) a complex-valued multiply-accumulate (MAC) unit, and(iii) a projection unit. For the bth PE, the gb-memory stores the bth row of the matrix G = (IB + γ −1AHA)−1, which we assume was computed during a separate preprocessing stage. A simulations are used to tune the parameter γ in order to improve the error-rate performance; the optimal value of γ depends on the antenna configuration. The complex-valued MAC unit is used by each PE to sequentially compute an entry of the output vector z(t+1)on line, while the entries of the vector x(t) are exchanged between the PEs in a cyclic fashion; this is done to avoid an architecture with a centralized x(t) memory that would suffer from a high fan-out because the memory's output has to be distributed to all the PEs. The projection unit implements the expansion-re projection operator proj(•) on line in a hardware-friendly manner. The outputs of the projection unit are also used to generate the quaternary outputs of the 1-bitprecoder; to this end, each PE simply takes the sign bits of the complex-valued output vector x(t+1).
In the first iteration (i.e., att = 1), each PE b is initialized with the bth entry of the vector x(1). Furthermore, the entries of the gb-memory are stored so that the first memory address corresponds to [G]b,b the second address to [G]b,b+1, and so forth (addresses wraparound). In the first clock cycle, each PE b computes [G]b, b[x(t)].

Proposed System
Process Of Mvm And Ecc

An idea based on ECC and MVM self-checking (checksum) for error protection of parallel MVM's in the MIMO systems. We assume real-time applications in which integer vectors come from ADCs with a fixed timing and processing is synchronous and repetitive, so a recomputation is not tolerable. This paper is an extension of that two page conference paper, and provides new results based on the FGPA implementation. To the best of the authors' knowledge, no other fault-tolerant design for parallel MVMs has been proposed for the MMO applications. In the proposed structure, a "detection matrix" D and a "sum matrix" A are added for fault tolerance. D is generated by performing ECC to the checksum row of each matrix, and A is a combination of all matrices under protection. By comparing the results of the original MVMs and that of the check matrix, the fault can be located. Then, the erroneous output vector can be recovered by subtracting the correct output vectors from the sum output vector.
Vector Method Of Detection Matrix And Sum Matrix

Assuming P different matrices Ap∈ ZN×M(p = 1, 2, . . . , P) (Z denotes integer domain) process in parallel an input vector . u∈ ZM×1, and generate P output vectors.zp ∈ ZN×1, the signal model for each MVM processing can be expressed as,

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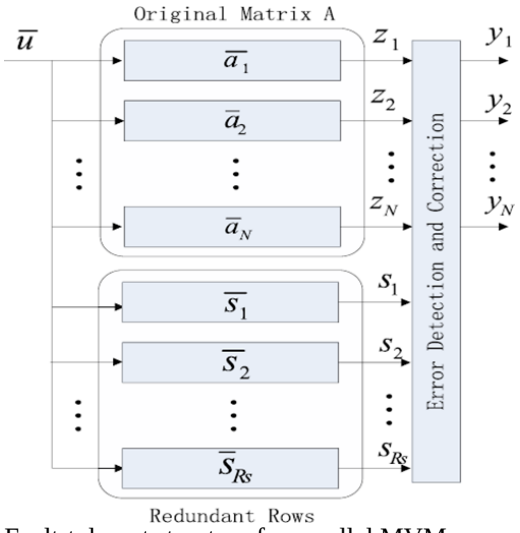
Ap × .u = z p, (p = 1, 2, . . . , P)….(4.2.1)

Due to radiation or any other interference, one or some branches of the parallel MVMs may not work correctly, so that some errors occur in the corresponding output vector. In this paper, the focus is on the case that there is a single error on one MVM, and it generates an output vector with erroneous elements. However, the ideas presented can be extended to tolerate multiple MVMs failures. The ECC approach can be applied to protect each of the MVMs.



Fault-tolerant structure for parallel MVMs

The above figure shows the fault-tolerant structure of the protection system, in which .an(n = 1, 2, . . . , N) are the rows of a matrix A, and Sr (r = 1, 2, . . . , Rs) are the redundant rows generated according to ECC approach . The constraint between the original output scalars zn (n = 1, 2, . . . , N) and the redundant outputs Sr (r = 1, 2, . . . , Rs) can be utilized in the error detection and correction module (ED and C) for outputting correct results yn (n = 1, 2, . . . , N). When a single error is considered (γ = 1), a Hamming code can be used for protection, and the relationship between N and Rs would be if the matrix has four rows (N = 4), a (7,4). Hamming code-based method can be used for the protection and the three redundant rows (Rs= 3) could be generated as s1’ = a1’ + a2’ + a3’ s2’ = a1’ + a2’ + a4’ s3’ = a1’ + a3’ + a4’.

Conclusion

The presence of hundreds of antenna elements at the base station (BS), however, results in excessively high hardware costs and power consumption, and requires high interconnect throughput between the baseband-processing unit and the radio unit. Massive MUMIMO that uses low-resolution analog-to-digital and digital-to analog converters (DACs) has the potential to address all these issues. In this project, a fault-tolerant design for parallel MVMs with new voting was proposed for the MIMO technology. The scheme combines the matrix self-checking (checksum) and the use of the error correction coding. We also presented a voting technique to recover multiple errors in MVM systems. In the proposed technique, we employed built-in design for test ability resources available in digital circuits to recover faulty modules in the presence of multiple transient faults. FPGA-based evaluation shows that the proposed scheme can reduce the overhead required compared to separate protection, for 4 and 8 parallel MVMs, respectively. This advantage would be larger for more parallel branches.

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