IJIRMET
ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering and Technology
Vol. 8, Issue 6, June 2023

The Usage of Dual Edge Triggered Flip-flops in Low Power, Low Voltage Applications

[1] S Soniya,[2] Dr.S.Lakshmi

[1] ME, Thirumalai Engineering College, Kanchipuram, India

[2] Associate professor, Department of ECE, Thirumalai Engineering College, Kanchipuram, India

[2] msklakshmi@gmail.com.

Abstract *In this paper, a novel low-power dual edge-triggered (DET) D-type flip-flop is proposed. This design achieves dual edge-triggered with two parallel data paths work in opposite phases of the clock single. Among them, a latch circuit structure employs differential input data signals which deposits very little capacitance on the clock line is accomplished. For fair comparison, four previously reported DET flipflops along with the proposed DETFF (DET flip-flop) are compared in terms of power consumption and power-delay product (PDP), under different data activities and different data rates. Several HSPICE simulation results show that the proposed DETFF is superior in power reduction at different parameters as compared to the existing DETFFs. Hence, the proposed DETFF is well suited for low power applications.*

KEYWORDS: *Single Edge-Triggered (SET), Dual Edge-Triggered (DET), Flip-Flop, Power Consumption, Power-Delay Product (PDP)*

1. INTRODUCTION

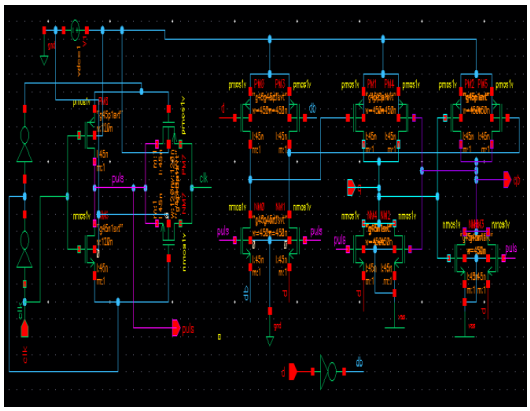
In many digital very large scale integration (VLSI) designs, the clock system that includes clock distribution network and flip-flops, is one of the most power consumption components. It accounts for 30% to 60% of the total system power, where 90% of which is consumed by the flip-flops and the last branches of the clock distribution network that is driving the flip-flop [1]. With the recent trend in frequency scaling and deep pipelining, this clocking system power may be even more pronounced. As the power budget of today's portable digital circuit is severely limited, it is important to reduce the power dissipation in both clock distribution networks and flipflops. Moreover, because of the tight timing budget at high frequency operation, the latency of the flip-flops should be minimized. Hence, the ability to achieve a design that ensures both power consumption and small latency is essential in modern VLSI technology. The dual-edge triggering is an important technique to reduce the power consumption in the clock distribution network. By utilizing dual-edge triggering, the flip-flop is capable of sampling data on both rising and falling edges of the clock so that only half the clock frequency is needed to obtain the same data throughput of single edgetriggered flip-flops (SETFFs) [2]. In deep sub-micron technology, the magnitude of power density becomes substantial and the coincident problems of heat removal and cooling are worsening. Low power gradually becomes one of the most important design considerations. In very large scale integration system (VLSI), clock network is one of the most power consuming components. The total 978-1-4799-3140-8/14/$31.00 ©2014 IEEE Kamal K. Kashyap Dept. Electronics and Communication National Institute of Technology, Kurukshetra Kurukshetra, India Kamalkant7185@gmail.com power dissipation of the clock network is given by following equation. Pelk = Voo 2 [felk (Celk + CfCelk) + fdata xCff _ data] (I) Where VDD is the supply voltage, fClk the clock frequency, fdata the average data frequency, Cclk the total capacitance related to the clock signal excluding flip-flops, CrcCIk the total capacitance related to the clock signal connected to the flipflops, and Cff _ data the total capacitance of the flip-flops connected to the data input. There are several ways to reduce clock power. The most influential way is V 00 scaling, which has quadratic impact on PcIk' However, Voo has already been reduced along with downscaling of process. The capacitance is unlikely to decrease as long as the number of transistors in a circuit becomes larger and functionality is more complex. One effective way to reduce fClk without performance degradation is to use dual edge-triggered flip-flops (DETFFs). The cross DETFF requires only half of felk to maintain the same throughput as single edge-triggered flip-flop (SETFF). Two main categories ofDETFFs are master slave and pulse triggered.

They put positive and negative flip-flops in parallel to perform dual edge triggering. These structures are straightforward. However, the internal are charging and discharging at every clock cycle regardless of the input even when they are sampled at the same value. This wastes a lot of power. Pulse triggered flip-flop is used for low power consumption. For rest of the paper, we organize our discussion in following manner. In section II, the previous work on dual edge triggered flip-flops (DETFF) is reviewed. Section III presents the structure and operating principal of proposed design. In section IV, simulation results are presented and in last, we draw conclusion in section V.

Review Of Exisisting Dual Edge Triggered Flip Flops

There are several ways to implement a double edge triggered flip flop. The first idea is to insert additional circuitry to generate internal pulse signals on each clock edge. The second idea is to duplicate the pathway to enable the flip flop to sample data on every clock edge [9]. Myint wai phyu et al. [3] has proposed dual edge triggered sense amplifier flip flop it consists of 3 stages shown in fig 1. They are pulse generator, sensing stage and the latching stage. The pulse generator generates the pulse at both the transition edges. The sensing stage is to reduce the time of signal propagation. For a sense amplifier based flip flops when input data is high RB will connect to Vdd and to be set to high. When data is low SB will connect to Vdd and to be set to high. In the latching stage there are two pulses controlled NMOS pass transistors these two can let D and DB feed to Q and QB directly this is the advantage of this structure. The disadvantage of this design is in the pulse generator two inverters are used to generate delay for the clock when the clock is from 0 to 1, because of the delay of the inverters clk2 cannot change from 0 to 1 immediately when clock gets to 1. If we use this pulse generator to drive more flip flops it possible that the magnitude of the pulse cannot get to the value which can open the NMOS in the sensing stage and latch. In the sensing stage of the flip flop when there is no pulse fed by the pulse generator and input data D is high point SB will be floating.

Fig.1.dual edge triggered sense amplifier flip flop.



Wang et al. [1] have proposed the transmission gated double edge triggered flip with 18 transistors. It is implemented by the idea of create duplicated pathway to enable the flip flop to sample data on every clock edge. It overcomes the problem of the yu's design. This design is implemented with transmission gates shown in fig2.two data paths are connected in parallel. The upper data path and lower data paths are triggered on the rising edge and falling edge of the clock signal respectively. An inverter and a PMOS transistors are used together to hold the logic level when the front transmission gate is closed. When the data value is low the inverter switches the signal to high which will isolate the data from Vdd and keep the value low. If the data value is high the inverter switches the signal to low which will make the PMOS transistor pull the data up to high.

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, June 2023

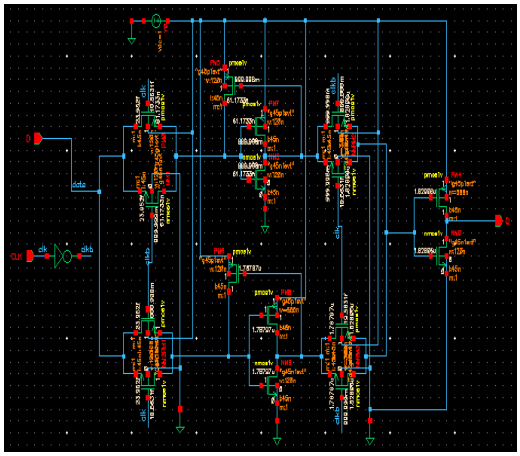


Fig.2. Transmission gated double edge triggered flip flop.

Tam et al. [2] have proposed design uses two flip flops and a multiplexer to implement a double edge triggered half static clock gated D type flip flop it is shown in fig 3.which consists of two dynamic master latches and a half static slave latch. It does not swap the use of master and slave latches in alternative clock phases to avoid the problem of coupling the half static latch directly to the input data path. A half static slave latch stores the data from each master latch in alternative clock phases.

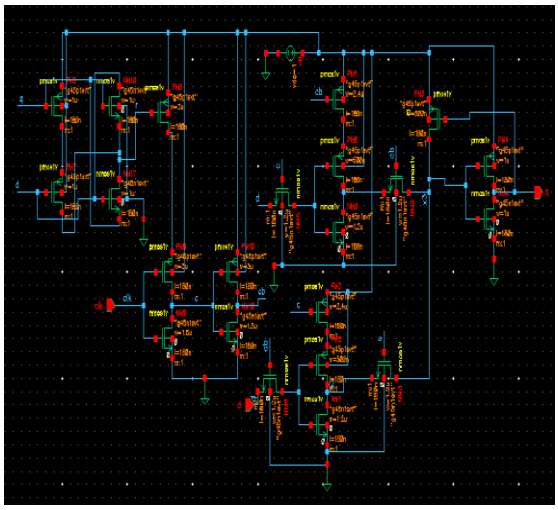


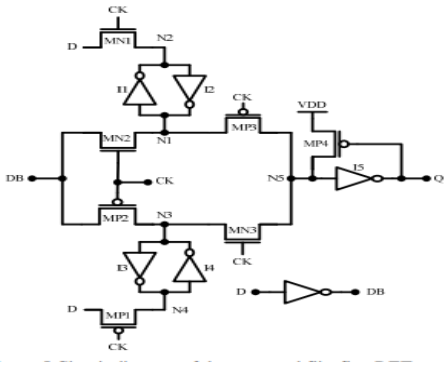
Fig.3. Double edge triggered half static clock gated D type flip flop.

When gated mode the gated clock signal r stays at 0 so if the input data changed when clk=0 then the value of C will change to 1 immediately. Asynchronous data sampling is caused when asynchronous clock edge of C triggers the flip flop. After each data transition the gated clock signal C goes back to 0 and stays low until the next transition.

Proposed Dual Edge-Triggered Flip-Flop

The proposed DET D-type flip-flop is illustrated. The proposed DETFF is composed of six pass transistors, two latches, and an output keeper circuit. Among them, the latches are respectively constructed by back-to-back configuration of inverters I1, I2 and inverters I3, I4; the output keeper circuit is formed by inverter I5 and regenerative transistor MP4. In the output near the supply voltage VDD when output terminal Q is at logic low.

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, June 2023



Proposed dual edge triggered flip flop.

This design also can be thought of as a parallel structure which similar to that of DETchung. Similarly, two differential master-slave flip-flops connected in parallel and each of flip-flop utilizes differential data signals at the master stage. As shown in Fig. 5, master latch can be further divided into sample portion and hold portion. The sample portion of the latch receives the differential data signals and passes them to the hold portion responsive to a control signal. However, the hold portion stores and outputs the differential data signals. In more detail, in the upper data path, the sample portion is for providing the differential data signals to hold portion when the clock signal is at logic high. The hold portion is for storing the differential data signals it receives from sample portion. A clock signal CK is provided to the gate terminal of both transistors MN1 and MN2. When the clock signal is at logic high, both transistors MN1 and MN2 are turned on. Conversely, when the clock signal is at logic low, both transistors MN1 and MN2 are turned off. The clock signal thus selects when the data signal D and the inverted data signal DB are passed to hold portion. The back-to-back configuration of inverters I1 and I2 stores the data signal D and the inverted data signal DB which are passed to hold portion. Finally, node N1 and node N2 provide the inverted data signal and the data signal, respectively, stored in hold portion. Besides, in the lower data path, master latch is essentially the same as that of the upper data path previously described, except transistors MP1 and MP2 are provided in place of transistors MN1 and MN2, respectively. Thus, sample portion provides the differential data signals to hold portion when the clock signal is at logic low. It is worth noting that, in this design, each data line in the sample portion comprises a single pass transistor for selectively passing one of the differential data signals responsive to the control signal, unlike that of DETchung which a tristate inverter is used.

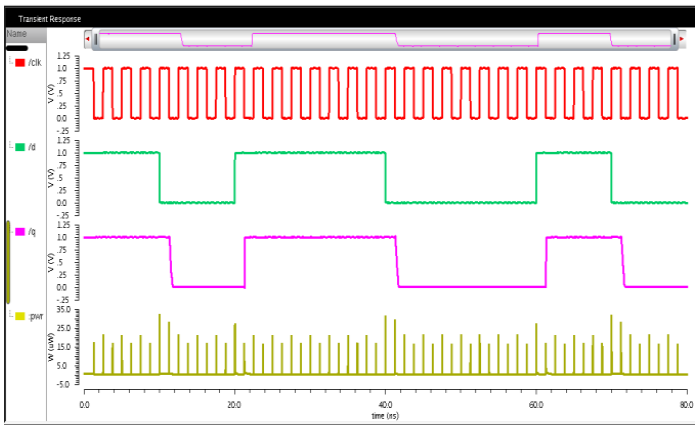
Simulation Results

Simulation has been done using the spectre simulator.

Design	Power(µw)	Delay(ns)	PDP(fJ)	Transistor count
Proposed	0.3013	1.265	0.3812	12
DETSAFF	3.033	0.45997	1.3950	20
T_DETFF	1.69	1.3174	2.2264	18
DHSCGFF	16.03	2.737	43.874	22

ISSN (Online): 2456-0448
International Journal of Innovative Research in Management, Engineering, and Technology
Vol. 8, Issue 6, June 2023

Comparison of Different Techniques



Wave form consist the clock (clk), data (d), output (q) and also power (pwr) signal.

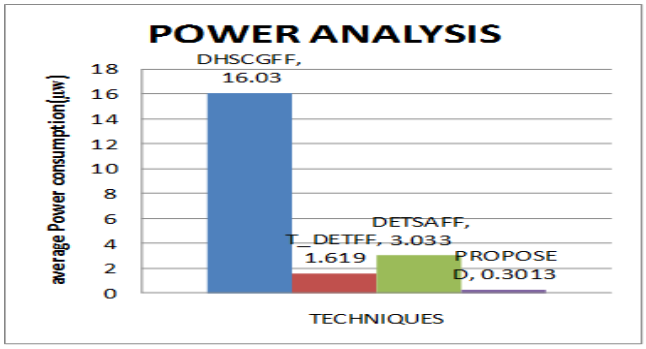
Wave form consist the clock (clk), data (d), output (q) and also power (pwr) signal. The following tables and graph shows the comparison of existing designs and the proposed design. From the comparison the proposed design consumes less power and less transistor count.The power consumption for different data inputs the average power consumption of the proposed design at different switching values. power consumption at different temperatures. From these tables transitions of the input data increases the power will also increased.The power analysis between the existing deigns and proposed designs.

Switching factor(α)	Data	Average power consumption(nw)
3	00001011	241.6
4	00011010	261
5	01011101	300.3
6	01010110	318.3
7	01010101	343.3

Average Power Consumption at Different

Temperatures for Different Techniques

Techniques → / Temperature(°c) ↓	T_DETFF Total Avg power(µw)	DHSCGFF Total Avg power(µw)	DETSAFF Total Avg power(µw)	Yu's Design Total Avg power(µw)	Proposed design Total Avg power(nw)
0	1.604	16.23	2.92	99.03	282.4
27	1.619	16.03	3.033	109.6	301.3
50	1.631	16.7	3.107	115.8	316.3
75	1.643	16.75	3.175	120.2	331.4
100	1.654	16.98	3.232	126.3	345.1



Comparison of power analysis graph

Conclusion

The proposed dual edge triggered flip flop is implemented for the low power applications. The structure of the proposed design has consist only 12 transistors which is less transistors than existing dual edge triggered flip flops. Based on obtained simulation results the proposed DET flip flop offers improvement in power dissipation and also less power delay product compared with existing systems.

Future Enhancement
As emerging technologies such as quantum computing and neuromorphic computing become more prevalent, integrating low-power DETFFs with these technologies can lead to improved energy efficiency and performance.
Developing tools for automated design of low-power DETFFs can enable faster and more efficient circuit design

REFERENCES

[1] H. Kawaguchi and T. Sakurai, "A reduced clock-swing flip-flop (RCSFF) for 63% power reduction," IEEE J. Solid State Circuits, vol.33, no. 5, pp. 807-811, May 1 998.
[2] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in Proc. 2002 Int. Symp. Low Power Electronics Design (ISPLED 2002), 2002, pp. 56-59.
[3] c.-c. Yu, "Design of low-power double edge-triggered flip-flop circuit," in Proc. 2nd IEEE Can! Industrial Electronics Applications (ICIEA 2007), May 2007, pp, 2054-2057.
[4] C. S, Kim, J. S. Kong, Y. S. Moon, and y, H. Jun, "Presetting pulse based flip-flop," in Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2008), May 2008, pp. 588-591.
[5] P. Zhao et al., "Low-power clock branch sharing double edge-triggered flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 3, pp. 338-345, Mar. 2007.
[6] P. Zhao, T. K. Darwish, and M. A. Bayoumi, "Highperformance and low-power conditional discharge flipflop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 1 2, no. 5, pp. 477-484, May 2004.
[7] B. S. Kong, S. S. Kim, and Y. H. Jun, "Conditionalcapture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, no. 8, pp. 1 263-1 271, Aug. 2001.
[8] M. W. Phyu, W. L. Goh, and K. S. Yeo, "A low-power static dual edge triggered flip-flop using an outputcontrolled discharge configuration," in Proc. IEEE Int. Symp. Circuits Systems (ISCAS 2005), May 2005, vol. 3, pp. 2429-2432.
[9] G. Aliakbar and M. Hamid, "Dual-edge triggered static pulsed flip-flops," in Proc. 18th Int. Conf. VLSI Design 2005, Jan. 2005, pp. 846-849.
[10] B. Nikolic, V. G. Oklobdzija, V. Stajanovic, W. Jia, 1. K. Chiu, and M. M. Leung, "Improved sense-amplifier based flip-flop: Design and measurements," IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 876-883, Jun. 2000.
[1 1] A. G. M. Strollo, D. De Caro, E. Napoli, and N, Petra, "A novel high speed sense-amplifier-based flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 1 1, pp. 1 266-1274, Nov. 200